Claims

[c1] A method for fabricating a gate structure for a semiconductor device, the gate structure being formed on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the method comprising the steps of :
removing material in a gate region of the device to expose a portion of the substrate;
forming a gate dielectric on the exposed portion of the substrate;
forming an inner spacer layer overlying the gate dielectric and the dielectric material;
forming a silicon layer overlying the inner spacer layer;
removing a first portion of the silicon layer and a first portion of the inner spacer layer, so that the top surface of the dielectric material is exposed and a second portion of the silicon layer and a second portion of the inner spacer layer remain in the gate region and have surfaces coplanar with said top surface; and
forming a silicide gate structure from the second portion of the silicon layer, the silicide gate structure being separated from the dielectric material by the second portion of the inner spacer layer.

[c2] A method according to claim 1, wherein the semiconductor device comprises a first gate region and a second gate region with an interface therebetween, and said step of forming an inner spacer layer further comprises covering said interface.

[c3] A method according to claim 1, wherein said step of removing material further comprises removing a hardmask overlying the gate region.

[c4] A method according to claim 1, wherein said step of removing material in the gate region forms a trench having sidewalls and a bottom, the bottom being the exposed portion of the substrate,
said step of forming the inner spacer layer further comprises forming said layer on the sidewalls of the trench, and
said step of forming the silicon layer comprises filling the trench

[c5] A method according to claim 1, wherein the semiconductor device is fabricated on a wafer, said step of forming the inner spacer layer comprises forming a blanket nitride layer on the wafer, and said step of forming the silicon layer comprises forming a blanket silicon layer on the wafer.

[c6] A method according to claim 1, wherein
the semiconductor device comprises a first gate region and a second gate region,
said removing steps and said forming steps are performed with respect to the first gate region, and
the method further comprises the steps of:
removing material in the second gate region of the device to expose a portion of the substrate;
forming a second gate dielectric on the exposed portion of the substrate;
optionally forming an additional inner spacer layer overlying the second gate dielectric and the dielectric material;
forming an additional silicon layer overlying the additional inner spacer layer and overlying the second gate dielectric;
removing a first portion of the additional silicon layer and a first portion of the additional inner spacer layer, so that the top surface of the dielectric material is exposed and a second portion of the additional silicon layer and a second portion of the additional inner spacer layer remain in the gate region; and
forming a second silicide gate structure from the second portion of the silicon layer, the second silicide gate structure being separated from the first silicide gate

structure by at least one of the inner spacer layer and the additional inner spacer layer.

[c7] A method according to claim 6, further comprising the step of depositing a metal layer overlying the silicide gate structure and the second silicide gate structure, thereby forming a contact to the silicide gate structure and the second silicide gate structure.

[c8] A method for fabricating a gate structure for a semiconductor device, the gate structure being formed on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the method comprising the steps of:
removing material in a gate region of the device to expose a portion of the substrate;
forming a temporary gate dielectric on the exposed portion of the substrate;
forming an inner spacer layer overlying the gate dielectric and the dielectric material;
removing the temporary gate dielectric and a first portion of the inner spacer layer, so that the top surface of the dielectric material is exposed and said portion of the substrate is exposed;
forming a new gate dielectric on said exposed portion of the substrate;
forming a silicon layer overlying the inner spacer layer

and overlying the top surface of the dielectric material;
removing a first portion of the silicon layer, so that the top surface of the dielectric material is exposed and a second portion of the silicon layer remains in the gate region and has a surface coplanar with said top surface; and
forming a silicide gate structure from the second portion of the silicon layer.

[c9] A method according to claim 8, wherein said step of removing material further comprises removing a hardmask overlying the gate region.

[c10] A method according to claim 8, wherein said step of removing material in the gate region forms a trench having sidewalls and a bottom, the bottom being the exposed portion of the substrate,
said step of forming the inner spacer layer further comprises forming said layer on the sidewalls of the trench, and
said step of forming the silicon layer comprises filling the trench.

[c11] A method according to claim 8, wherein the semiconductor device is fabricated on a wafer, said step of forming the inner spacer layer comprises forming a blanket nitride layer on the wafer, and said step of forming the

silicon layer comprises forming a blanket silicon layer on the wafer.

[c12] A method according to claim 10, wherein the first portion of the inner spacer layer is removed by a directional etching process, so that a second portion of the inner spacer layer remains on the sidewalls of the trench.

[c13] A method according to claim 12, wherein the directional etching process removes a portion of the inner spacer layer at an upper portion of the sidewalls of the trench.

[c14] A method according to claim 8, wherein the semiconductor device comprises a first gate region and a second gate region with an interface therebetween, and said step of forming an inner spacer layer further comprises covering said interface.

[c15] A semiconductor device having a gate structure on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the device comprising:
a gate dielectric overlying a portion of the substrate in a gate region and in contact therewith;
an inner spacer layer in contact with the dielectric material; and
a silicide structure having an upper surface coplanar with said top surface,

wherein the gate region is characterized as a trench having a bottom and sidewalls, the gate dielectric overlies the bottom of the trench, the inner spacer layer is in contact with the sidewalls of the trench, and the silicide structure fills the trench.

[c16] A semiconductor device according to claim 16, wherein the inner spacer layer overlies the gate dielectric and is in contact therewith.

[c17] A semiconductor device according to claim 15, wherein the gate region has disposed therein a first silicide structure and a second silicide structure, and a portion of said inner spacer layer separates the first silicide structure and the second silicide structure.

[c18] A semiconductor device according to claim 17, further comprising a metal layer overlying the first silicide structure and the second silicide structure and in contact therewith.

[c19] A semiconductor device according to claim 15, wherein the inner spacer layer comprises
silicon nitride.

[c20] A semiconductor device according to claim 17, wherein the gate region includes a first portion and a second portion, the first portion having disposed therein a first

inner spacer and the first silicide structure and the second portion having disposed therein a second inner spacer and the second silicide structure, so that at a boundary between the first portion and the second portion a portion of the first inner spacer and a portion of the second inner spacer are in contact.